REMARKS

EXAMINER INTERVIEW SUMMARY

A telephonic Examiner Interview was conducted on February 13, 2008 with Examiner Chun Kuan Lee, Examiner's supervisor Alfred Kindred and Applicant's representative Amir A. Tabarrok. The objection to drawings was discussed. More particularly, the objection to Figure 1 was discussed. As a result, there was an agreement and the objection to drawings has withdrawn.

Moreover, the use of Figure 1 as allegedly Applicant Admitted Prior Art (AAPA) was discussed. As a result, an agreement was reached to withdraw the rejections based on Figure 1.

Claim Rejections 35 U.S.C. 112

Claims 1-22 are rejected, under 35 U.S.C. 112, first paragraph, as allegedly failing to comply with the enablement requirement. Applicant respectfully traverses in view of the following.

For example, the instant application discloses that by issuing the start up command upfront, at the beginning of the disk transaction, the system can immediately begin the start up process of the disk drive mechanism (see Instant Application, page 11, lines 19-21). The startup delay of the disk drive can be typically four to six microseconds (see Instant Application, page 11, lines 21-22). Once the startup command is issued by the processor to the disk controller, the

Attorney Docket No. NVID-P000817 Serial No. 10/725,980 Page 8

Examiner: Lee, C. Art Unit: 2182

processor uses the startup delay time to prepare the disk transaction information by packaging a plurality of data structures comprising the disk transaction (see Instant Application, page 11 line 24 to page 12 line 1). The startup process has not completed since the delay time is used to prepare the disk transaction information.

Accordingly, the recited limitation is supported by the specification. As such, independent Claims 1, 9 and 14 are in compliance with 35 U.S.C. §112, first paragraph. Thus, withdrawal of the rejection is earnestly solicited.

Dependent claims are in compliance with 35 U.S.C. §112, first paragraph, by virtue of their dependency and withdrawal of the rejection is similarly requested.

Claim Rejections 35 U.S.C. 103

Claims 1-22 are rejected, under 35 U.S.C. 103(a), as being allegedly unpatentable by Applicant's Admitted Prior Art (AAPA) in view of Wilcox (U.S. 6,185,634) (hereinafter Wilcox). Applicant respectfully traverses in view of the following.

Independent Claim 14 recites

"a processor;

a system memory coupled to the processor;

a bridge component coupled to the processor; and

a disk controller coupled to the bridge component, the disk controller including a plurality of bypass registers, wherein the processor executes software code stored in the system memory, the software code causing the computer system to implement a method comprising:

upon receiving a request for a disk I/O from an application executing on the computer system, transferring a command from the processor to the disk

Attorney Docket No. NVID-P000817 Serial No. 10/725,980 Page 9

Examiner: Lee, C. Art Unit: 2182

controller, the command causing a start up of a disk drive coupled to the disk controller:

subsequent to transferring the command causing the start up and before the completion of said start up, preparing disk transaction information by packaging a plurality of data structures comprising the disk transaction;

transferring the disk transaction information to the bypass registers of the disk controller; and

implementing a disk I/O, wherein the disk controller processes the disk transaction information to control the disk drive."

As presented and discussed above, the rejection based on the alleged AAPA of Figure 1 has been withdrawn pursuant to the Examiner Interview referenced above. Thus, a processor, a system memory, a bridge component, and a disk controller, as claimed are not shown by the cited combination.

The cited portion of the alleged AAPA discloses that a DMA transfer from the system memory to the disk controller is used to implement the disk transaction (see Instant Application, page 4, lines 11-13). For example, the preparation of a disk transaction includes generating and arranging transaction information, e.g., PRDs, wherein the transaction information is loaded to system memory (see Instant Application, page 4, lines 13-18). A pointer is used to access system memory and retrieve the disk transaction information and that once the disk controller has the necessary transaction information, the disk controller issues commands to start up the disk drive mechanism and implement the disk transaction (see Instant Application, page 4, lines 20-24). Problems, however, remain with respect to excessive amount of latency and overhead within the ADMA disk transaction methodology (see Instant Application, page 4, lines 26-27).

Examiner: Lee, C.

Art Unit: 2182

Attorney Docket No. NVID-P000817 Page 10 Serial No. 10/725,980

The alleged AAPA fails to either teach or suggest preparing disk transaction information by packaging a plurality of data structure comprising the disk transaction, in the claimed fashion. For example, the alleged AAPA discloses that the preparation for a disk transaction retrieves all the necessary disk transaction information and then issues a command to start up the disk drive mechanism whereas independent Claim 14 recites subsequent to transferring the command causing the startup and before the completion of the startup, preparing disk transaction, as claimed. Thus, the alleged AAPA fails to teach or suggest that subsequent to transferring the command causing the startup, and before the completion of the startup, preparing disk transaction information by packaging a plurality of data structures comprising the disk transaction, as claimed.

Moreover, the alleged AAPA <u>teaches away</u> from the claimed limitation because of the excessive amount of latency and overhead. Moreover, the alleged AAPA <u>teaches away</u> by teaching that the startup command is not issued until all the necessary disk transactions are retrieved that lead to an excessive amount of latency and overhead.

Thus, not only does the alleged AAPA fail to teach or suggest that subsequent to transferring the command causing the startup and before the completion of the startup, preparing disk transaction information by packaging a plurality of data structures comprising the disk transaction, as claimed, but the alleged AAPA teaches away because of problems associated with the excessive

Attorney Docket No. NVID-P000817 Page 11 Serial No. 10/725,980

Examiner: Lee, C. Art Unit: 2182

amount of latency and overhead. Under similar rationale, the alleged AAPA fails to either teach or suggest the recited limitations and in fact <u>teaches away</u> from transferring the disk transaction information to the bypass registers of the disk controller; and implementing a disk I/O, wherein the disk controller processes the disk transaction information to control the disk drive, as claimed.

The rejection admits that the alleged AAPA fails to teach "upon receiving a request for a disk I/O from ...; subsequent to transferring the command causing the startup ...; and the disk controller including a plurality of bypass registers ...". The rejection relies on Wilcox. Applicant respectfully traverses.

Wilcox discloses that when in the idle state, a first signal is asserted, thereby coupling a multiplexer to the first source address signal from the source address register to the second input terminal of the first adder (see Wilcox, col. 11, lines 41-46). Wilcox further discloses that the adder adds a size parameter to the first address (see Wilcox, col. 11, lines 48-49). Moreover, Wilcox discloses that the address generated by the first adder is the memory address of the end of the first sector's worth of data and that when this address is generated during the DMA transfer, there is sufficient data in the memory for a sector to be written to the disk drive (see Wilcox, col. 11, lines 52-56).

Accordingly, Wilcox discloses how the address is generated when a start signal is asserted. However, Wilcox fails to either teach or suggest that

Examiner: Lee, C.

Art Unit: 2182

Attorney Docket No. NVID-P000817 Page 12 Serial No. 10/725.980

subsequent to transferring the command causing the startup <u>and before the</u> completion of the startup, preparing disk transaction information, as claimed.

Furthermore, Wilcox discloses a memory component within a disk adapter (see Wilcox, Figure 1, element 56 and col. 3, lines 35-40). A memory component, as disclosed by Wilcox, fails to teach or suggest a plurality of bypass registers, as claimed.

Accordingly, the alleged AAPA alone or in combination with Wilcox fails to render independent Claim 14 obvious, under 35 U.S.C. §103(a). Independent Claims 1 and 9 recite limitations similar to that of Claim 14 and are patentable for similar reasons. Dependent claims are patentable by virtue of their dependency.

As per Claims 2-5, 7-8, 10-11, 13, 15-17 and 19-20, Applicant respectfully asserts that the alleged AAPA <u>cannot</u> be used as a prior art reference for reasons discussed above.

As such, allowance of Claims 1-22 is earnestly solicited.

For the above reasons, Applicant requests reconsideration and withdrawal of the rejections under 35 U.S.C. §112 and 35 U.S.C. §103.

Examiner: Lee, C.

Art Unit: 2182

CONCLUSION

In light of the above listed remarks, reconsideration of the rejected Claims 1-22 is requested. Based on the arguments presented above, it is respectfully submitted that Claims 1-22 overcome the rejections of record and, therefore, allowance of Claims 1-22 is earnestly solicited.

Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Dated: Feb 14th, 2008

Respectfully submitted, MURABITO, HAO & BARNES LLP

Amir A. Tabarrok
Registration No. 57,137

MURABITO, HAO & BARNES LLP Two North Market Street Third Floor San Jose, California 95113

Examiner: Lee, C.

Art Unit: 2182